

DUPLEX LCD DRIVER

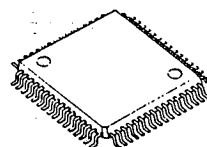
■ GENERAL DESCRIPTION

The NJU6432B is a duplex LCD driver to drive segment type LCD panel.

2-common and 53-segment drivers can drive up to 104 segments.

The NJU6432B is useful for the Digital Tuning System or others segment type display driver.

■ PACKAGE OUTLINE

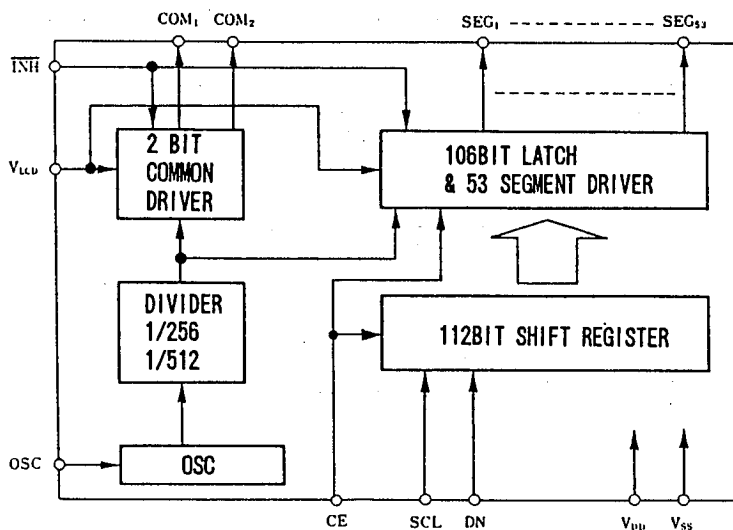


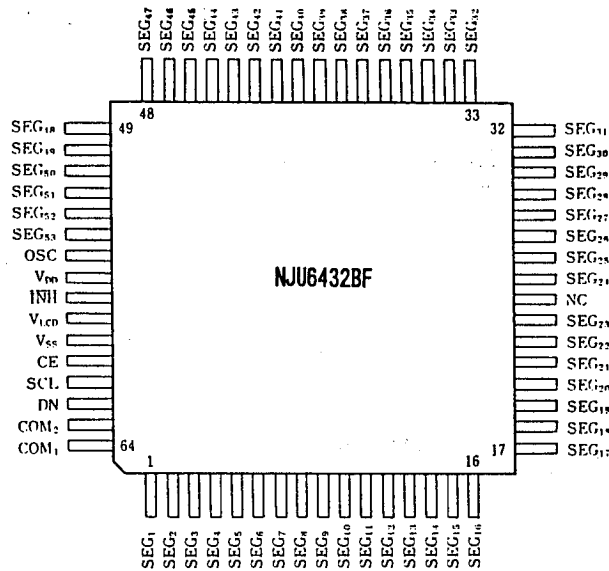
■ FEATURES

- 53 Segment Drivers
- Duty Ratio 1/2 ;104-Segment Drive
- Serial Data Transmission (Shift Clock 2MHz max.)
- Display Off Function (INH Terminal)
- Operating Voltage — 6.5V Max.
- Package Outline — QFP 64
- C-MOS Technology

NJU6432BF

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1~23 25~53	SEG ₁ ~ SEG ₂₃ SEG ₂₄ ~ SEG ₄₃	Segment Output Terminal
54	SEG ₅₃	Normally On Segment Output Terminal (When the "L" level input to the INH terminal, this segment also turns off.)
55	OSC	Oscillating Terminal
56,59	V _{DD} , V _{SS}	Power Supply
57	INH	Display-Off Control Terminal: When "L" level input to this terminal, all of the display turns off including SEG ₅₃ .
58	V _{LCD}	Power Supply for LCD Driving
60	CE	Chip Enable Terminal
61	SCL	Serial Data Transmission Clock Terminal
62	DN	Serial Data Input Terminal
63 64	COM ₂ COM ₁	Common Output Terminal.
24	NC	Non Connection

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuits

Oscillation by connecting external resistor and capacitor.

This circuits supply the basical clock signal to other circuits like as common driver and segment driver.

(1-2) Driving Circuits

This circuit divide the oscillating frequency by 1/256 and 1/512, and generate the common and segment output timing signals.

(1-3) Shift-Register

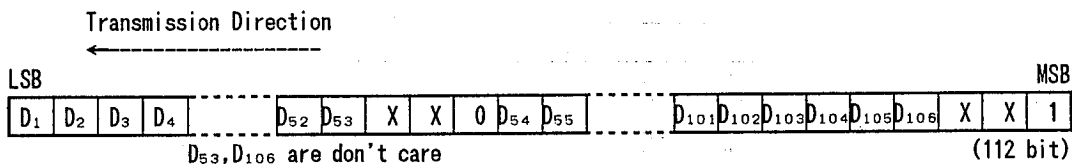
During the CE signal is "H", the data input to this shift-register by synchronizing the shift clock.

(1-4) Latch and Segment Driver

During the CE signal is "L", the data in the shift-register transfer to the latch and the segment driver output the LCD driving waveform according to the latched data.

(2) Data Input Format (The Data Correspond to the Output)

(2-1) Data Input Format



(2-2) Input Data Correspond to Segment Status

Data Dxxx	Segment Status
"H"	ON
"L"	OFF

(2-3) Input Data Correspond to Segment Terminals

Segment	Data	COM ₁	COM ₂
SEG ₁	D ₁	○	
	D ₂		○
SEG ₂	D ₃	○	
	D ₄		○
SEG ₃	D ₅	○	
	D ₆		○
SEG ₂₆	D ₅₁	○	
	D ₅₂		○
SEG ₂₇	D ₅₄	○	
	D ₅₅		○
SEG ₄₉	D ₉₈	○	
	D ₉₉		○
SEG ₅₀	D ₁₀₀	○	
	D ₁₀₁		○
SEG ₅₁	D ₁₀₂	○	
	D ₁₀₃		○
SEG ₅₂	D ₁₀₄	○	
	D ₁₀₅		○
SEG ₅₃	ON	○	
	ON		○

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage	V _{DD}	- 0.3 ~ + 7.0	V
Operating Voltage	V _{LCD}	- 0.3 ~ V _{DD} +0.3	V
Input Voltage (1)	V _{IN}	- 0.3 ~ + 7.0	V
Input Voltage (2)	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Output Voltage (2)	V _O	- 0.3 ~ V _{DD} +0.3	V
Output Current (3)	I _O	100	μA
Output Current (4)	I _O	1.0	mA
Power Dissipation	P _D	300	mW
Operating Temperature	T _{opr}	- 30 ~ + 85	°C
Storage Temperature	T _{stg}	- 40 ~ + 125	°C

- * 1) CE, SCL, DN Terminals
- * 2) OSC Terminal during OFF-output
- * 3) SEG₁~SEG₅₃ Terminals
- * 4) COM₁,COM₂ Terminals

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=-30~+85°C. VDD=6.5V, VSS=0V)

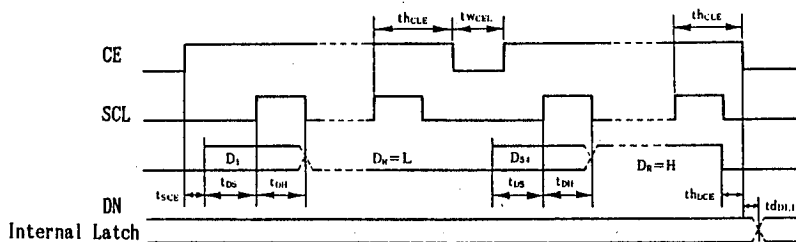
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	VDD	VDD Terminal	2.5		6.5	V
Supply Voltage	VLCD	VLCD Terminal	2.5		VDD	V
Operating Current	IDD	VDD Terminal			1	mA
Operating Current	ILCD	VLCD Terminal			2	mA
"H" Input Voltage	VIH	TNH Terminal	0.7VDD		6.5	V
"L" Input Voltage	VIL	TNH Terminal	0		0.3VDD	V
"H" Input Voltage	VIH	CE,SCL,DN Terminals	0.8VDD		6.5	V
"L" Input Voltage	VIL	CE,SCL,DN Terminals	0		0.2VDD	V
Oscillator Resistor	ROSC	OSC Terminal		51		kΩ
Oscillator Capacitor	COSC	OSC Terminal		680		pF
Oscillator Frequency	fOSC	OSC Terminal	25	50	100	kHz
"H" Input Current	IIH	VIN=6.5V, CE, SCL,DN,TNH Terminals			5	μA
"L" Input Current	IIL	VIN=0V, CE, SCL,DN,TNH Terminals			5	μA
"H" Output Voltage	VOH	IO=-10μA SEG1~SEG53 Terminals	VLCD-1.0			V
"L" Output Voltage	VOL	IO=10μA SEG1~SEG53 Terminals			1.0	V
"H" Output Voltage	VOH	IO=-100μA COM1,COM2 Terminals	VLCD-0.6			V
"L" Output Voltage	VOL	IO=100μA COM1,COM2 Terminals			0.6	V
Middle Level Voltage	VMID	IO=±100μA,VLCD=6.5V	2.65	3.25	3.85	V
		IO=±100μA,VLCD=3.0V	0.9	1.5	2.1	
Hysteresis Voltage	VH	VDD=5V, CE,SCL,DN Terminals	0.3			V

AC Characteristics

 $(T_a = -30 \sim +85^\circ\text{C}, V_{DD} = 6.5\text{V}, V_{SS} = 0\text{V})$

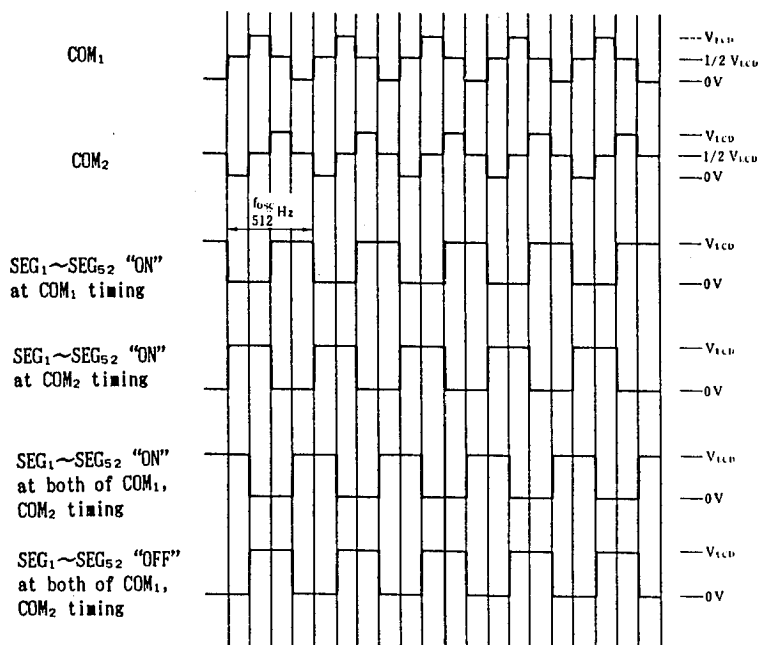
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL Terminal	0.25			μs
"H" Clock Pulse Width	t_{WCLH}	SCL Terminal	0.25			μs
Data Set-up Time	t_{DS}	SCL, DN Terminals	0.25			μs
Data Hold Time	t_{DH}	SCL, DN Terminals	0.25			μs
CE Set-up Time	t_{SCE}	CE, DN Terminals	1			μs
CE Hold Time (1)	t_{HDCE}	CE, DN Terminals	1			μs
CE Hold Time (2)	t_{HCE}	CE, SCL Terminals	1.25			μs
Data Latch Delay Time	t_{DLP}				1	μs
"L" Clock Enable Pulse Width	t_{WCEL}	CE Terminal	4			μs

• Input Timing Characteristics

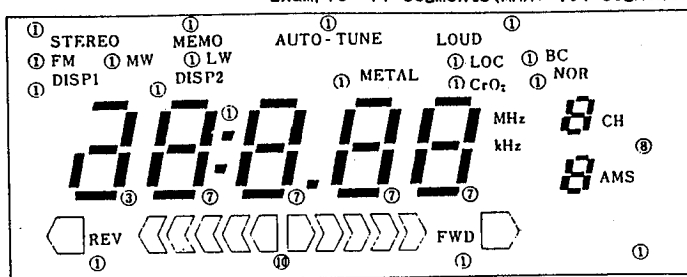


The data is latched at $D_R=H$ and falling edge of the CE signal condition.

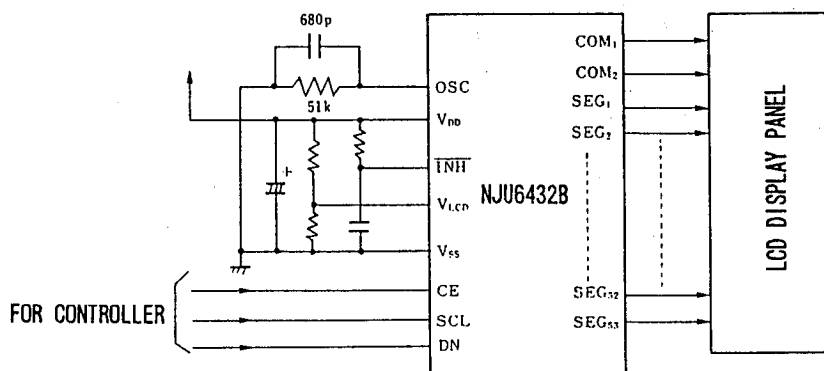
• Output Timing Characteristics



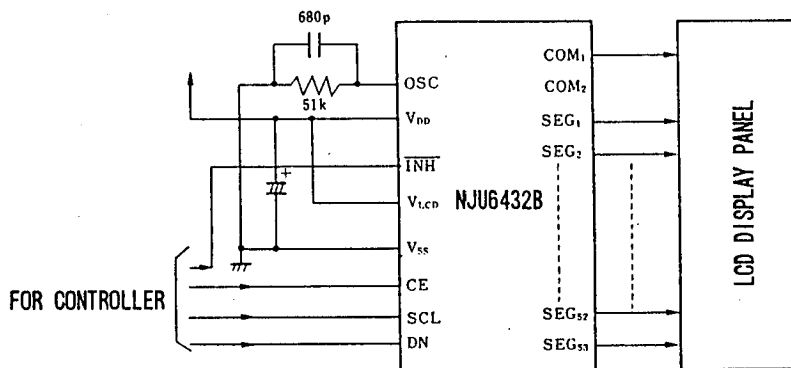
Example: 71 segments(MAX. 104 segments)



① In case of $V_{LCD} < V_{DD}$



② In case of $V_{LCD}=V_{DD}$



(Note) After rising edge of V_{DD} voltage, the display data is not guaranteed and which blinking is meaningless display. Therefore, keep $\overline{TNH}$ terminal to Low Level by the display data transferred is needed.

MEMO

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